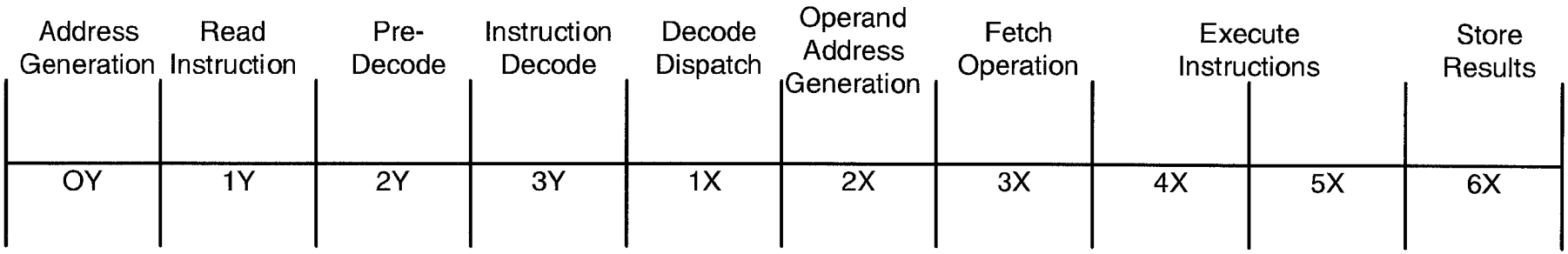


FIG. 1

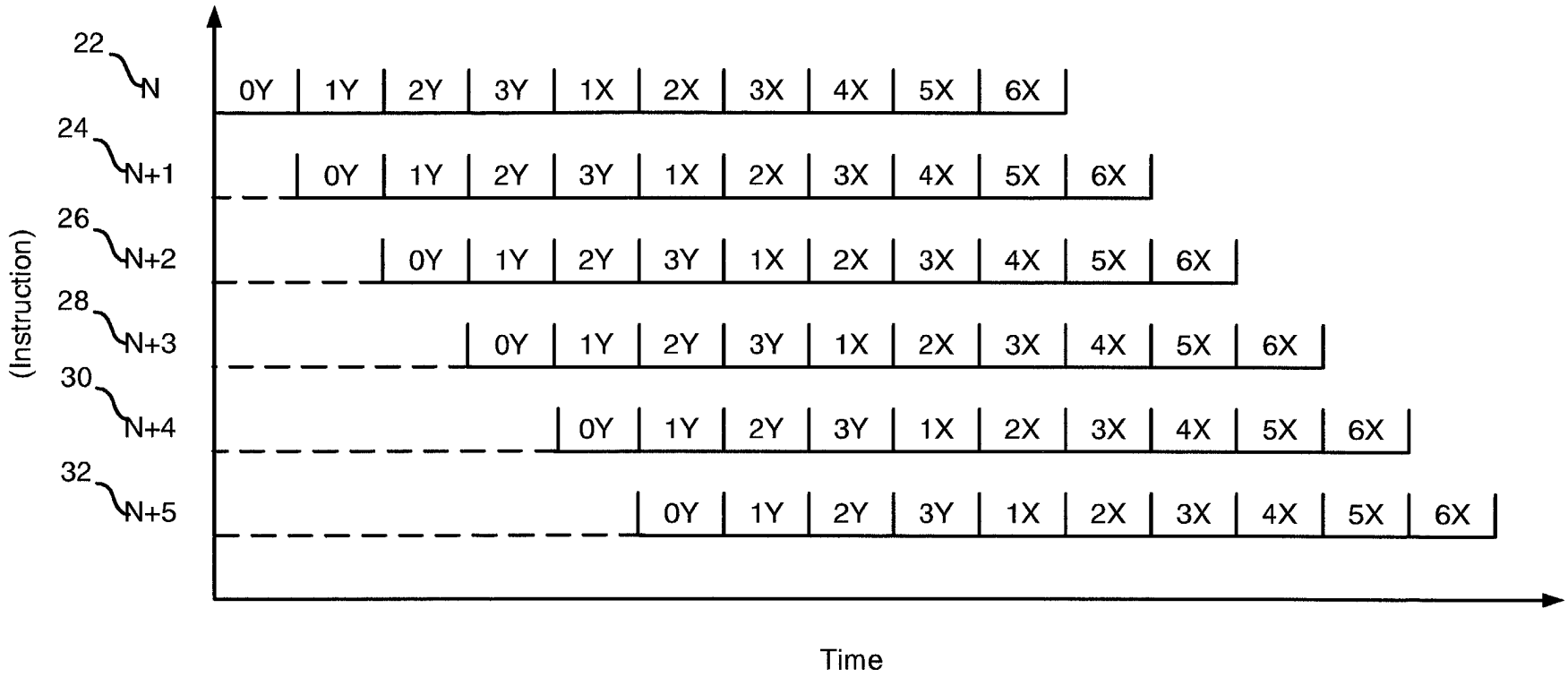


FIG. 2

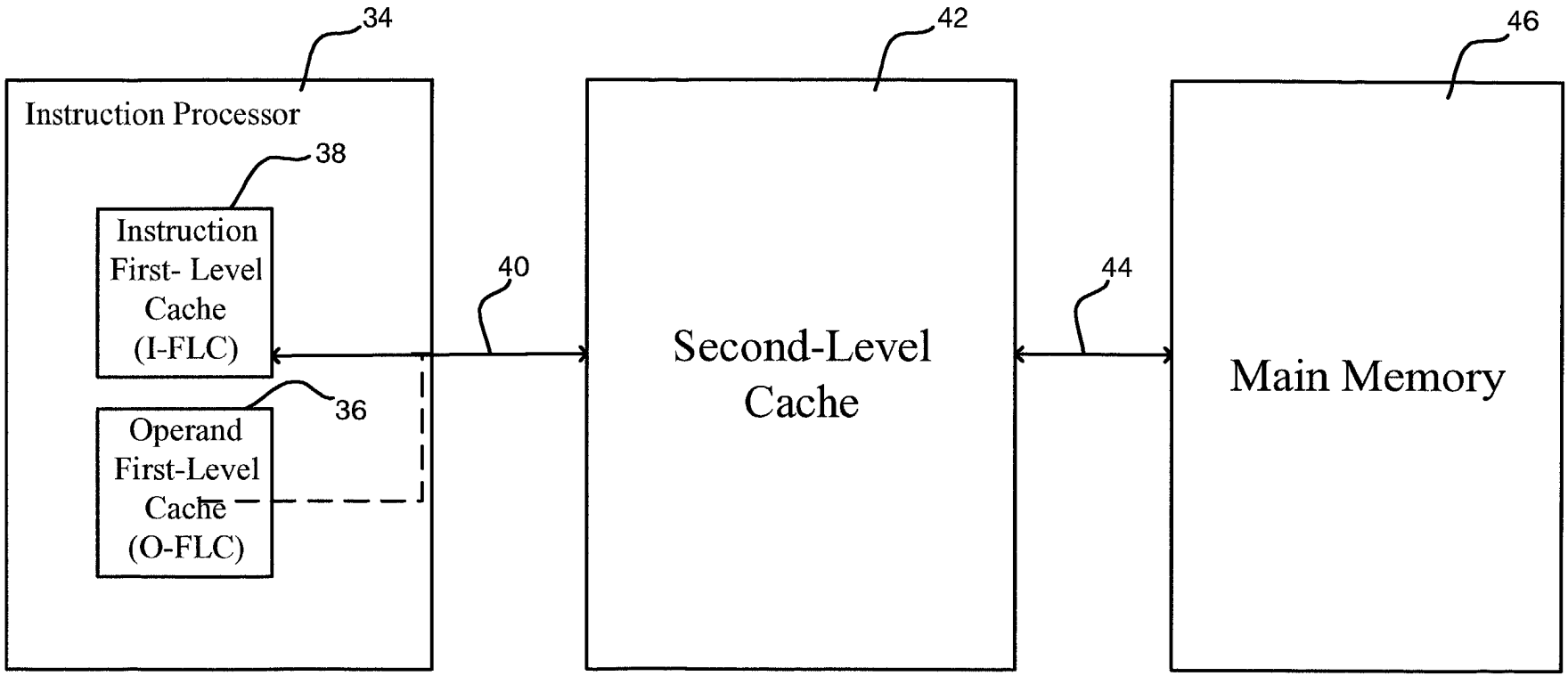

34
Instruction Processor
38
Instruction First- Level Cache (I-FLC)
36
Operand First-Level Cache (O-FLC)
40
42
Second-Level Cache
44
46
Main Memory

FIG. 3

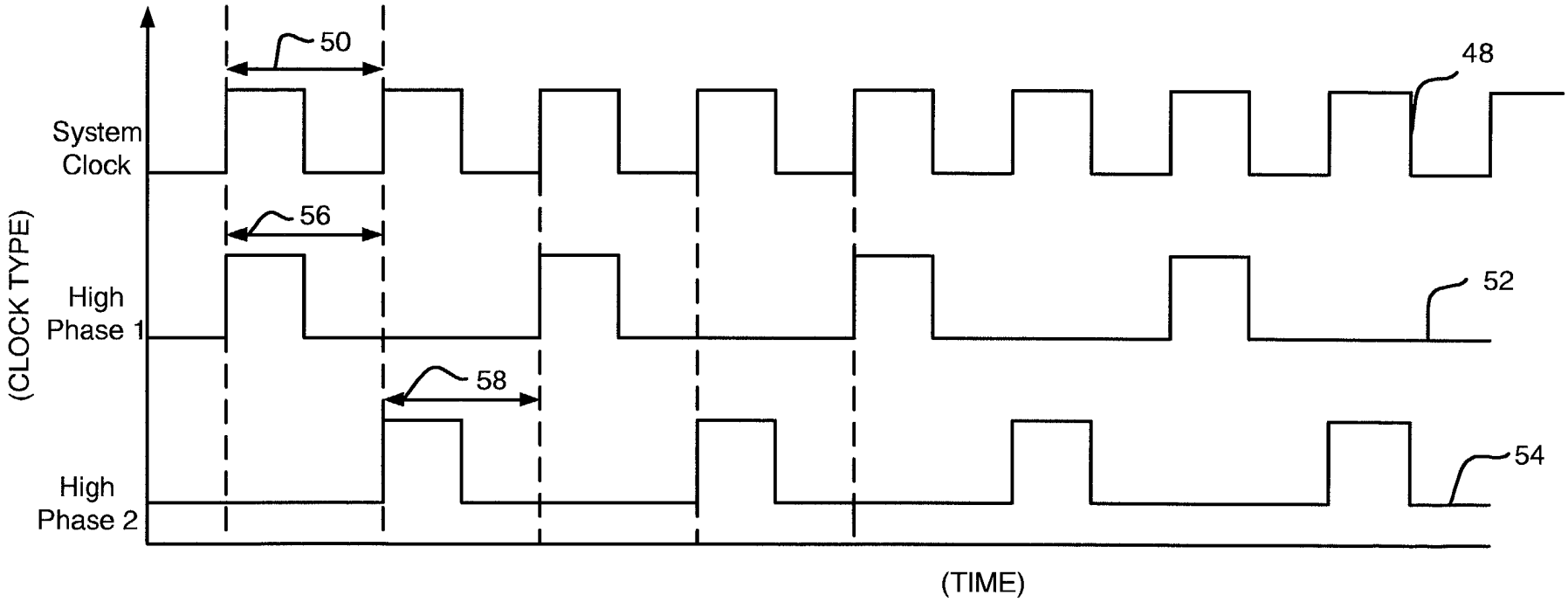


FIG. 4

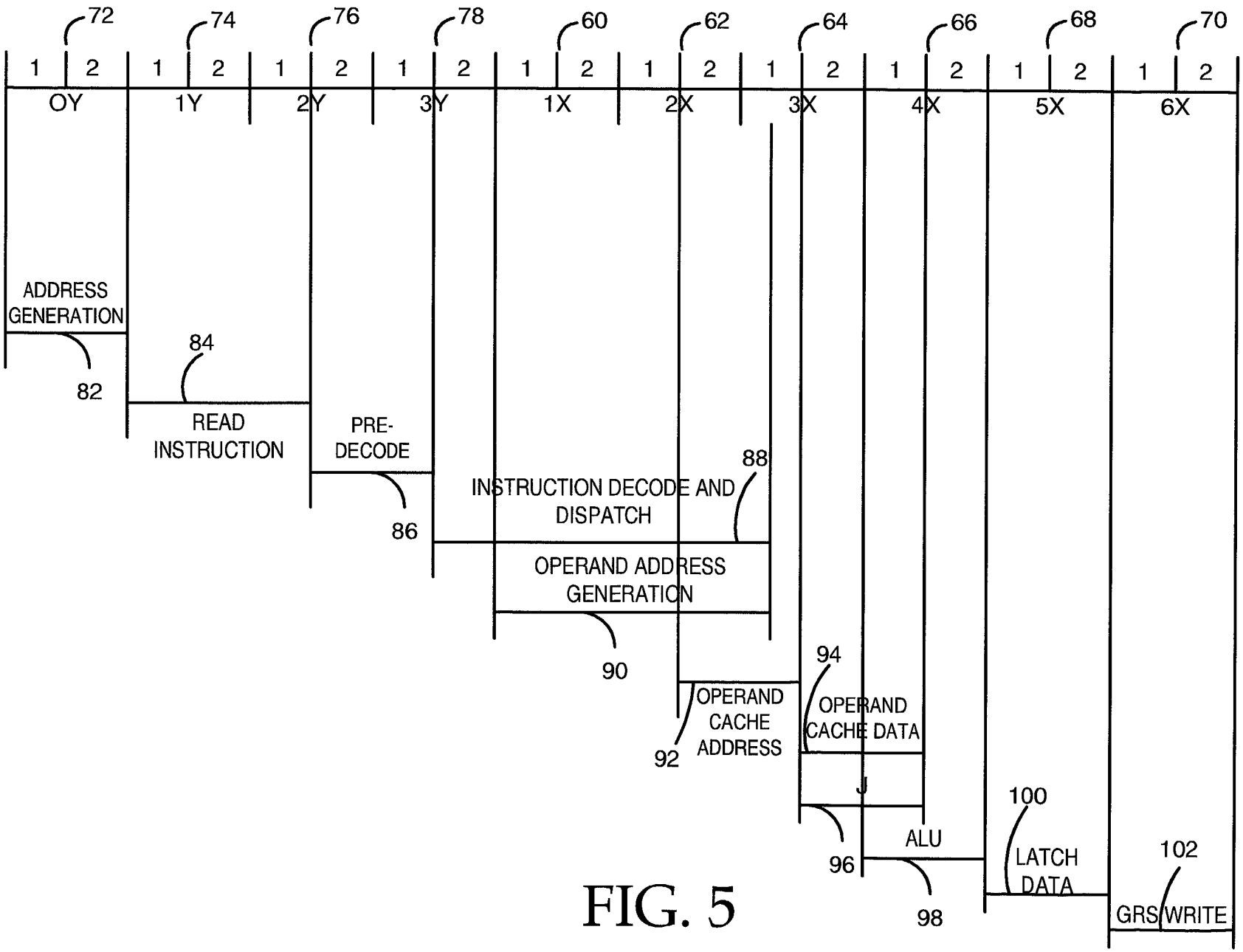

72
74
76
78
60
62
64
66
68
70
1 2 1 2 1 2 1 2 1 2 1 2 1 2 1 2 1 2 1 2
OY
1Y
2Y
3Y
1X
2X
3X
4X
5X
6X
ADDRESS GENERATION
82
84
READ INSTRUCTION
PRE-DECODE
86
88
INSTRUCTION DECODE AND DISPATCH
OPERAND ADDRESS GENERATION
90
92
OPERAND CACHE ADDRESS
94
OPERAND CACHE DATA
J
96
ALU
98
100
LATCH DATA
102
GRS WRITE

FIG. 5

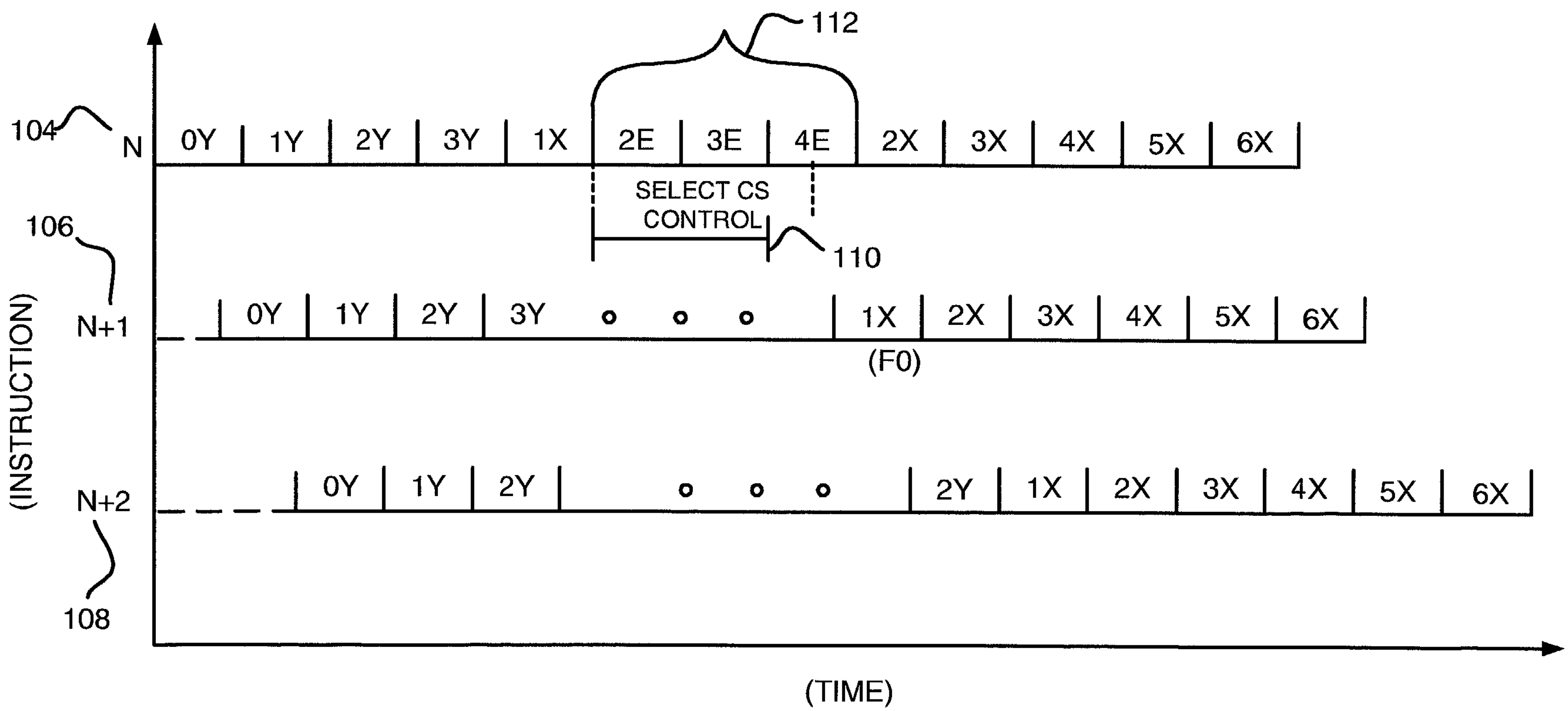

112
104
N
0Y
1Y
2Y
3Y
1X
2E
3E
4E
2X
3X
4X
5X
6X
SELECT CS CONTROL
110
106
N+1
0Y
1Y
2Y
3Y
1X
2X
3X
4X
5X
6X
(F0)
(INSTRUCTION)
N+2
0Y
1Y
2Y
2Y
1X
2X
3X
4X
5X
6X
108
(TIME)

FIG. 6

FIG. 7

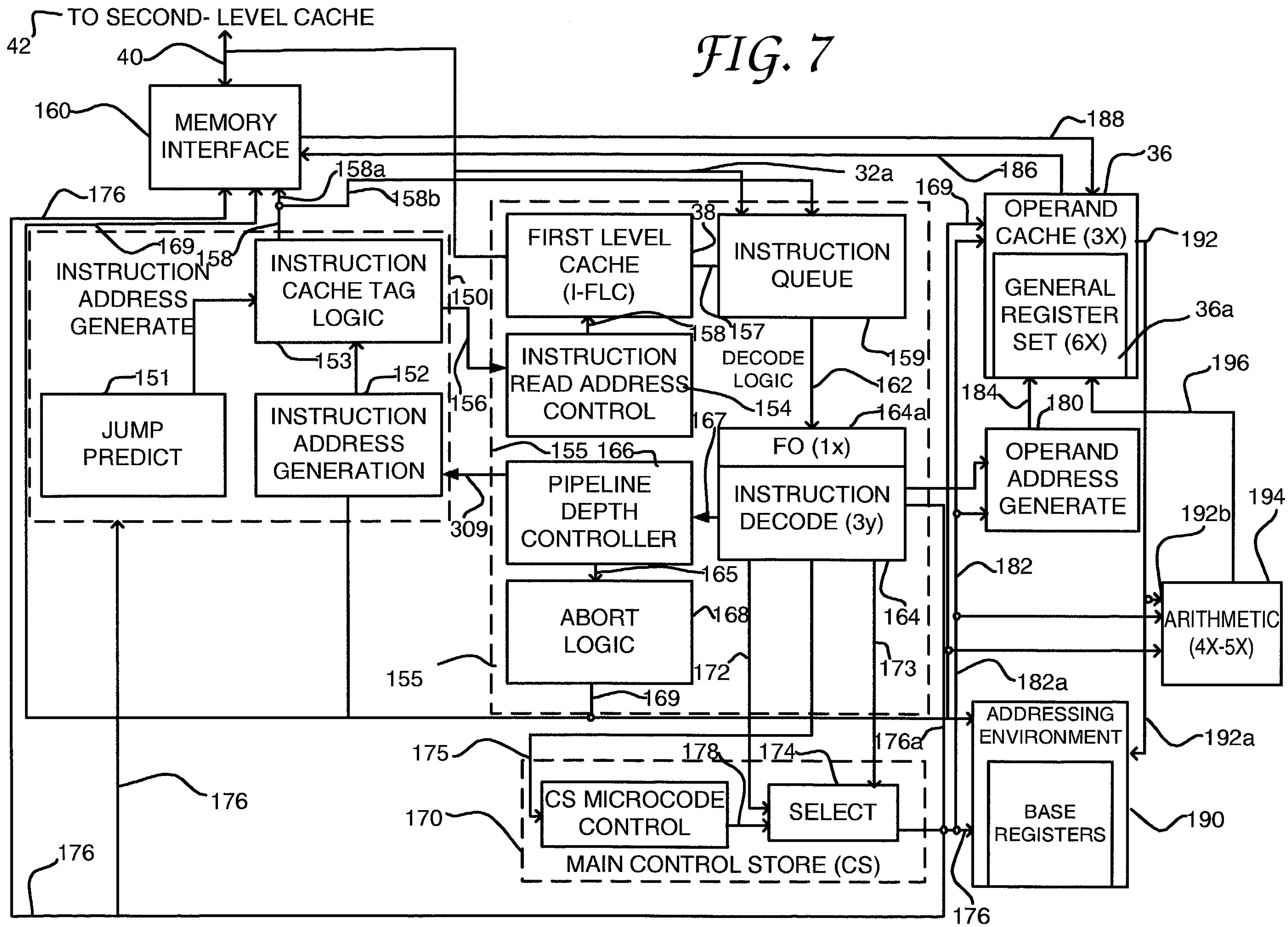
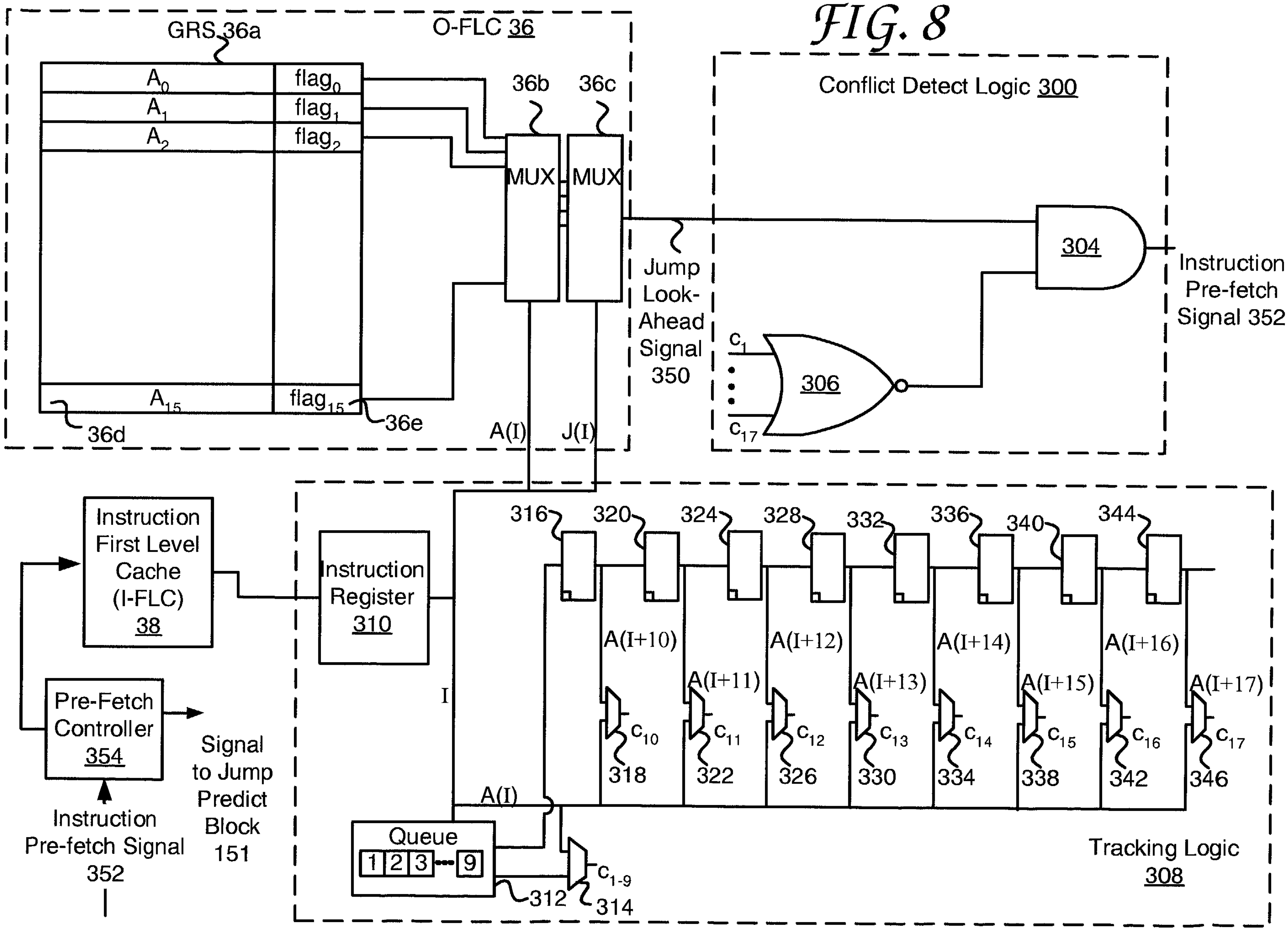

TO SECOND- LEVEL CACHE
42
40
160
MEMORY INTERFACE
158a
158b
176
169
158
INSTRUCTION ADDRESS GENERATE
INSTRUCTION CACHE TAG LOGIC
150
153
151
152
JUMP PREDICT
INSTRUCTION ADDRESS GENERATION
156
309
FIRST LEVEL CACHE (I-FLC)
38
INSTRUCTION QUEUE
32a
158
157
159
DECODE LOGIC
162
INSTRUCTION READ ADDRESS CONTROL
154
164a
167
FO (1x)
INSTRUCTION DECODE (3y)
155
166
PIPELINE DEPTH CONTROLLER
165
ABORT LOGIC
168
164
172
173
169
155
175
178
174
176a
CS MICROCODE CONTROL
SELECT
170
MAIN CONTROL STORE (CS)
176
176
176
188
186
169
36
OPERAND CACHE (3X)
192
GENERAL REGISTER SET (6X)
36a
196
184
180
OPERAND ADDRESS GENERATE
182
192b
194
ARITHMETIC (4X-5X)
182a
ADDRESSING ENVIRONMENT
192a
BASE REGISTERS
190

FIG. 8


GRS 36a
O-FLC 36
A0
A1
A2
A15
flag0
flag1
flag2
flag15
36b
36c
MUX
MUX
36d
36e
A(I)
J(I)
Jump Look-Ahead Signal 350
Conflict Detect Logic 300
304
306
c1
c17
Instruction Pre-fetch Signal 352
Instruction First Level Cache (I-FLC) 38
Instruction Register 310
Pre-Fetch Controller 354
Signal to Jump Predict Block 151
Instruction Pre-fetch Signal 352
I
316
320
324
328
332
336
340
344
A(I+10)
A(I+11)
A(I+12)
A(I+13)
A(I+14)
A(I+15)
A(I+16)
A(I+17)
c10
c11
c12
c13
c14
c15
c16
c17
318
322
326
330
334
338
342
346
A(I)
Queue
1 2 3 9
c1-9
312
314
Tracking Logic 308

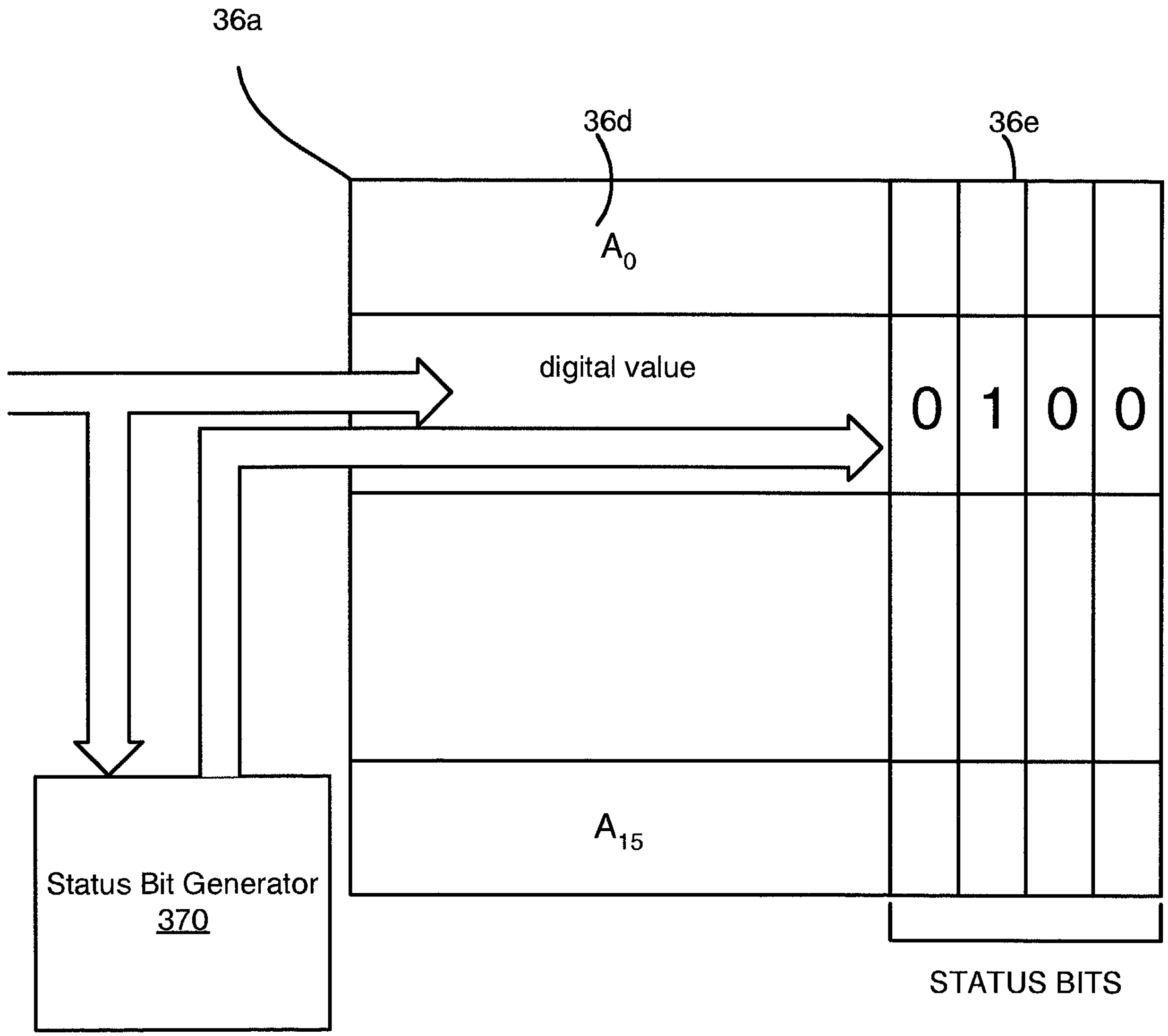

36a
36d
36e
A0
digital value
0
1
0
0
A15
Status Bit Generator
370
STATUS BITS

FIG. 9